High-Pass Lumped-Element Transmission Lines

Danny R. Webster, *Member, IEEE*, Gholam-Reza Ataei, *Student Member, IEEE*, and David G. Haigh, *Senior Member, IEEE*

***Abstract*— In this letter the high-pass lumped-element transmission line is shown to have a number of useful advantages over the classic low-pass line including dc isolation between sections, lower loss per section, and a much higher maximum frequency of operation, far beyond the natural self-resonant frequencies of the passive components used.**

***Index Terms*— Microwave integrated circuits, MMIC's, transmission lines.**

I. Introduction

A LOW third-order intermodulation distortion amplifier design technique called "Derivative Superposition" [1] requires the parallel connection of FET's with different gate bias voltages in a 50-Ω environment. The "Distributed Amplifier" approach [2]–[5] would provide good broadband impedance matching and has the useful ability to absorb the field-effect transistor (FET) capacitances into the transmission line structure (whether implemented with lumped or distributed elements). But the technique does not provide dc isolation between the FET's.

The ideal solution would be a transmission line structure that provides the impedance matching property, while simultaneously providing dc isolation. This can be achieved by performing the low-pass to high-pass transformation on the classic low-pass lumped-element transmission line.

In this letter we describe a prototype high-pass lumped-element transmission line designed with surface-mount components. We show how the self-resonance behavior of the individual components can be exploited to extend the useful bandwidth far beyond the self-resonant frequencies of the individual components used. Next we present measured results for the prototype line. Finally we explore the potential of high-pass transmission lines in monolithic microwave integrated circuit (MMIC) form.

II. Implementing High-Pass Transmission Lines with Real Components

A section of an ideal lumped-element low-pass transmission line is shown in Fig. 1(a). In a classic distributed amplifier, the FET would be connected to the mid node, and its port capacitance can be absorbed into C. It inherently provides dc coupling between the input and output of the section. By carrying out a low-pass to high-pass transformation on the T-section in Fig. 1(a), it is possible to derive its ideal high-pass equivalent [Fig. 1(b)], which has the same characteristic impedance. This topology provides dc isolation between the input and the output of the line. DC bias for an FET connected to the mid node can be supplied via the ground connection of the inductor with suitable decoupling.

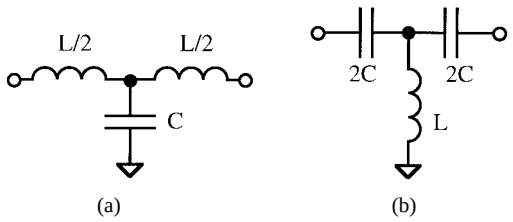

Fig. 1. Lumped-element transmission line T-sections. (a) Low pass. (b) High pass.

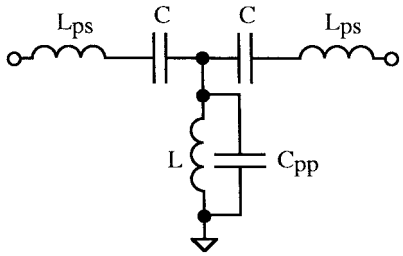

Fig. 2. Realistic model of the high-pass transmission line T-section.

In practice, real inductors have parasitic parallel capacitance ($C_{\rm pp}$), and real capacitors have parasitic series inductance ($L_{\rm ps}$). This leads to an equivalent circuit for the high-pass T-section of Fig. 2. At low frequencies, it can be argued that L and C are the dominant components, and the structure behaves as a high-pass transmission line. However, at high frequencies, $L_{\rm ps}$ and $C_{\rm pp}$ are now the dominant components within the circuit, and subsequently form a parasitic low-pass transmission line. Thus the overall structure has a band-pass response. If both lines do not have the same characteristic impedance (i.e., within 10% of Z_o), significant pass-band ripple will occur.

In order to minimize the pass-band ripple, L and C must be chosen (or designed), such that their parasitic components satisfy the following relationship:

$$Z_o = \sqrt{\frac{2L}{C}} \approx Z_{\rm op} = \sqrt{\frac{2L_{\rm ps}}{C_{\rm pp}}} \tag{1}$$

where Z_o is the characteristic impedance of the high-pass transmission line, and $Z_{\rm op}$ is the characteristic impedance of the parasitic low-pass transmission line. For low group delay

Manuscript received August 13, 1997. This work was supported by the Engineering and Physical Sciences Research Council (U.K.).

The authors are with the Department of Electronic and Electrical Engineering, University College London, Torrington Place, London, WC1E 7JE, U.K.

Publisher Item Identifier S 1051-8207(98)00855-1.

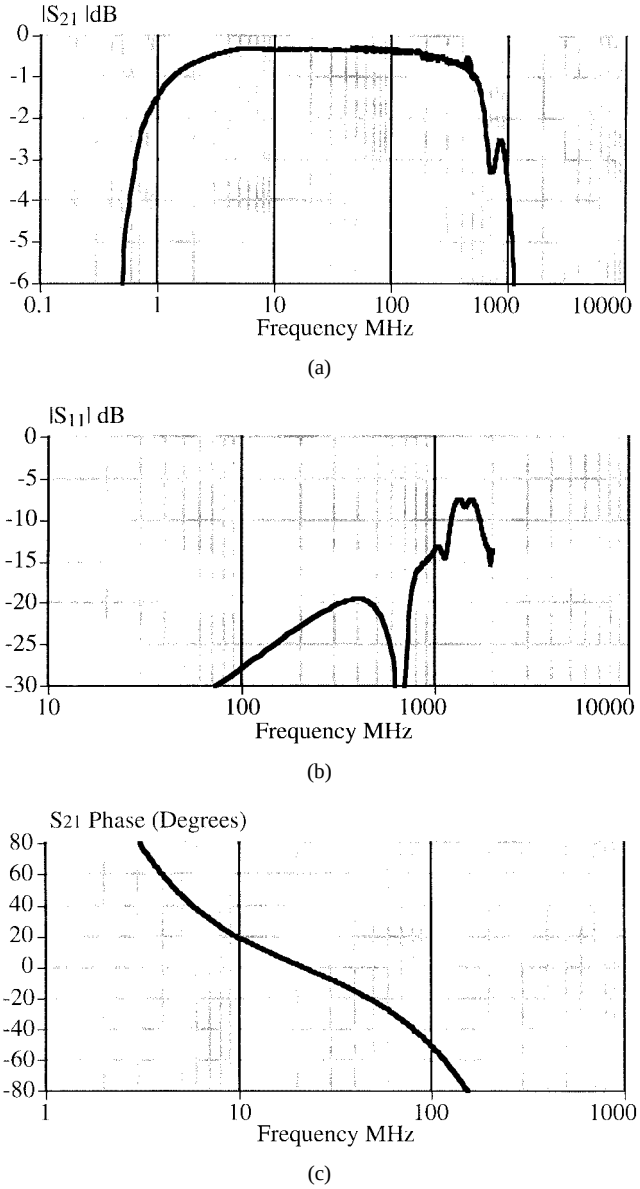

Fig. 3. Measured (a) $|S_{21}|$ (b) $|S_{11}|$ (c) phase of S_{21} of a five-section surface mount lumped-element high-pass transmission line.

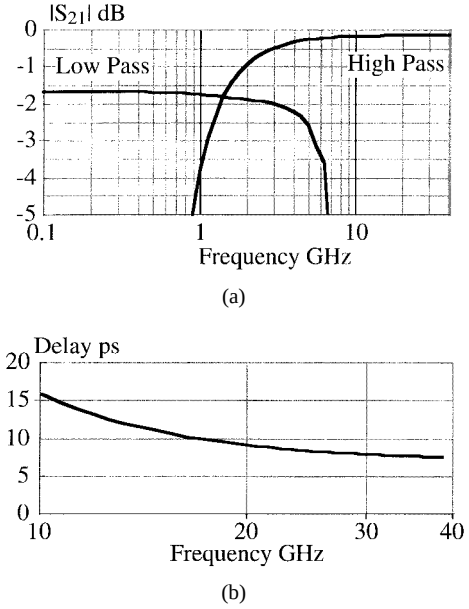

Fig. 4. (a) Simulated $|S_{21}|$ for five-section low-pass and high-pass transmission lines using lumped-element models of MMIC inductors and capacitors. (b) Simulated group delay for high-pass line.

across the center of the passband and maximum bandwidth, it is necessary for $L \gg L_{\rm ps}$. A possible advantage of the high-pass structure is that the relatively lossy inductor is now in the high impedance shunt branch rather than in the low-impedance series branch, reducing the loss of the line. There is also some scope for absorbing FET intrinsic capacitance into the parasitic capacitance $C_{\rm pp}$ of the inductor L.

III. Measured Performance of Prototype High-Pass Transmission Line

A prototype five-section line was designed using SPICE with approximate parasitic models for Murata LQ1H series surface mount inductors and X7R dielectric surface mount ceramic capacitors. Values of $L = 10\ \mu$H and $C = 8.2$ nF were chosen to give a parasitic line impedance $Z_{\rm op}$ close to 50 Ω. A prototype board was constructed and its components characterized. The measured parasitics were found to be $C_{\rm pp} = 3.3$ pF and $L_{\rm ps} = 5$ nH, corresponding to self resonance frequencies of 27.7 and 24.9 MHz, respectively, giving a $Z_{\rm op}$ of 54.8 Ω. If required, the parasitic inductance $L_{\rm ps}$ (or the parasitic capacitance $C_{\rm pp}$) could have been increased to equalize $Z_{\rm op}$ to Z_o [see (1)].

In Fig. 3. we show the measured s-parameter behavior of the prototype line. This design has a bandwidth of about three decades spanning from 700 kHz to 700 MHz. (A higher bandwidth would have been possible for a higher L.) The insertion loss of the line is 0.06 dB per section. The design has a good return loss up to about 1 GHz showing a good approximation to a 50-Ω match over its working bandwidth. The circuit also shows a low rate of change of phase shift with frequency in the mid band region (circa $\pm 50^\circ$ between 4.5–100 MHz).

IV. Projected Performance of MMIC High-Pass Lines

In this section we simulate the potential performance of a high-pass lumped-element transmission line implemented with typical MMIC components and compare it to a comparable low-pass line. The simulations use MMIC library models for a 40 GHz process which are valid up to about 40 GHz.

The low-pass line was designed to give the highest possible cutoff frequency by using the smallest spiral inductor in the MMIC foundry library. This had a value of 1 nH with 2 Ω of series resistance and a self-resonant frequency of 40 GHz. This required a capacitance of 0.8 pF to achieve a 50 Ω line.

The high-pass line was designed to give the lowest possible cutoff frequency by using the largest spiral inductor in the library. This had a value of 7 nH with 5.5 Ω of series resistance and a self-resonant frequency of 11 GHz. This required a capacitance of 5.6 pF with 34 pH of parasitic inductance to achieve a 50-Ω line in both the high-pass mode

and the parasitic low-pass mode. The metalization loss of the capacitor and associated parasitic inductance is estimated from the foundry guide to be 0.15 Ω.

In Fig. 4(a) we show the comparison of the simulated five-section MMIC high-pass and low-pass lines. It can be seen that the high pass line has a bandwidth from 1 GHz to at least 40 GHz, with very low loss (0.2 dB) around 10 to 40 GHz due to metalization loss. It can be seen that the low-pass line achieves a bandwidth from dc to about 7 GHz with 1.8-dB loss at 1 GHz due to inductor loss. The simulations suggest that the low-pass line could also have a parasitic high-pass mode that could lead to a spurious pass band above 200 GHz. Despite using an inductor with a higher loss and a lower self-resonant frequency, the high-pass line had a lower loss and a higher frequency range than the low-pass line. In Fig. 4(b) we show the group delay of the high-pass line between 10 and 40 GHz.

V. Conclusion

A lumped-element demonstrator of the high-pass transmission line has been built and measured. It gave low insertion loss and good return loss over nearly three decades of frequency. It also possessed low group delay over a decade of frequency.

The high-pass line has a number of advantages over the classic low-pass line including dc isolation between sections, lower insertion loss, and a higher maximum frequency of operation, far beyond the natural self-resonant frequency of the passive components used. The high-pass line is similar to the classic low-pass line as it gives a broadband impedance match, and when used in a distributed amplifier topology, it can absorb capacitance from FET devices into the transmission line.

The high-pass line would appear potentially useful for thin-film hybrid and millimeter-wave MMIC work, where there is good control and repeatability of the magnitude of parasitic components.

As well as "Derivative Superpostion" circuits, the high-pass line may also be useful for amplifiers with digitally controllable gain.

References

[1] D. R. Webster, J. B. Scott, and D. G. Haigh, "Control of circuit distortion by the derivative superposition method," *IEEE Microwave Guided Wave Lett.*, vol. 6, pp. 123–125, Mar. 1996.

[2] W. S. Percival, "Thermionic valve circuits," British Patent 460562, July 1936.

[3] C. S. Aitchison, "The intrinsic noise-figure of the MESFET distributed-amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. 33, pp. 460–466, June 1985.

[4] I. D. Robertson, Ed., *MMIC Design*. London, U.K.: The Institution of Electrical Engineers, 1995.

[5] A. Borjak, P. Monteiro, I. Z. Darwazeh, and J. J. Oreilly, "Multigigabit distributed-amplifiers for signal shaping applications," *Electron. Lett.*, vol. 32, no. 4, pp. 355–356, 1996.